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## “The Location of Technological Innovations within the Japanese Semiconductor Industry”

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## **The Location of Technological Innovations within the Japanese Semiconductor Industry.**

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### ***1. Introduction***

Much of the current literature on hi-tech developments within the electronics industry tends to focus on the spatial and organisational arrangements evident in innovative clusters such as Silicon Valley. There are, however, many very different forms of spatial organisation which engender innovations within the semiconductor industry, and these variations depend on the particular sub-sector of the semiconductor industry. In this paper we discuss the case of Japanese vertically integrated semiconductor producers. The paper will analyse data from over 100 semiconductor firms located in Japan. In particular, we will focus on the firms undertaking the wafer manufacturing processes. Our results indicate that the spatial arrangements here are very different from those evident in the US or Europe. As we will see in this paper, in order to discuss the geographical behaviour of many parts of the semiconductor industry, it is necessary to consider not only organizational issues, but also the different sub-sectors within the industry. From these perspectives, many of the generalizations made about the semiconductor industry based on observations of Silicon Valley are seen to be rather inappropriate.

The paper is organized as follows. In section 2 we review the types of arguments frequently associated with discussions about the spatial organization of the semiconductor industry and spatial patterns of innovation. In section 3, we describe the three different components of the semiconductor industry. As we will see, many of the issues raised in section 2 really only relate to one sub-sector of the electronics industry, and the two other parts of the industry have been almost entirely ignored in the literature. In section 4 we discuss the Japanese wafer-processing sub-sector of the industry, and using very detailed indices of product innovations, we estimate relationships between geographical, firm and technological variables within a product-cycle framework. We find very little support for a product-cycle type model. In order to account for these findings we explore the organizational issues governing the spatial patterns of product innovations within Japanese industry.

### ***2. Geography and the Semiconductor Industry***

Over the last decade there has been a significant growth in interest in the geographical behaviour of firms in the electronics and semiconductor industry (Oakey and Cooper 1989; Saxenian 1994; Almeida and Kogut 1997; Kittiprapas and McCann 1999). There are a variety of interrelated reasons for this recent research interest, which can broadly be grouped into three themes. The first theme is a general renewal of academic interest in geography and industrial location issues per se. This has been encouraged in part by the continuing process of economic integration in many parts of the world, such as the EU and

NAFTA, as well as by the writings of certain influential commentators (Porter 1990; Krugman 1991). The second theme is a growth in interest in the particular characteristics of the electronics and semiconductor industry itself. The reason for this is partly that electronics, and in particular the semiconductor part of the electronics industry, is generally regarded as an industry which is both highly successful, and also at the forefront of human technological development (Piore and Sabel 1984; Best 1990). At the same time, innovations in this industry are often embodied into the production technology of other industries, thereby having induced productivity effects. Therefore, it is implicitly assumed that observation of the behaviour of the electronics and semiconductor sector may also provide clues as to the future trajectory of other industrial sectors in general. A third reason for the growth in interest in the electronics and semiconductor industry has been the apparent tendency of this industry to cluster in particular locations such as Silicon Valley (Scott 1988, 1991; Saxenian.1994; Angel 1991). The result of this behaviour is that certain areas appear to exhibit high growth performance in this sector, while other areas have been unable to develop any equivalent industry base (*The Economist* 1997). This has led to concern among public policy planners in various countries and regions (Castells and Hall 1994) to understand the economic-environmental conditions under which such industrial clusters are fostered, in the hope of replicating these conditions elsewhere.

In order to generate such an array of new product developments, these combined features are assumed to imply that the semiconductor industry will also tend to be at the forefront of organizational developments (Eisenhardt and Schoonhoven 1990) and production process innovations (McCann and Fingleton 1996). Therefore, observation of the current organizational behaviour of the semiconductor industry may point towards the future behaviour of industry in general, as other industrial sectors attempt to imitate the successful organization and production innovations exhibited by this sector. Indeed, much of the current thinking about the optimal relationship between industry organization and geography has been developed on the basis of observations of the large numbers of small and medium sized semiconductor firms in locations such as Silicon Valley (Saxenian 1994; Scott 1988, 1991; Larsen and Rogers 1984). In many circles (Keeble and Wilkinson 1998) it has now become almost a matter of faith that many small and medium sized firms clustered at the same location will guarantee the maximum levels of product innovation (Aydalot and Keeble 1988; Saxenian 1994). The logic behind this argument is that such small firms are assumed to find it not only relatively easy to share information and to benefit from local information spillovers, but also to reconfigure their organizational and input-output linkages appropriately as new product developments occur. Empirical support for these arguments, which appears to confirm the local presence of industry-specific informal information spillovers, comes primarily from patent citation counts (Jaffe et al. 1993; Almeida and Kogut 1997). Meanwhile, these observations of the high growth performance of small firm clusters such as Silicon Valley (Saxenian 1994), Cambridge UK (Castells and Hall 1994) and Ile de France (Scott 1988) are contrasted with the relatively weaker growth performance of the large-firm parts of the electronics industry (Saxenian 1994). Explanations for the apparent difference in the growth performance of the small and large firm sectors, are based on the assumptions that the organizational rigidity and well-defined boundaries of large hierarchical firms, limit the ability of large firms to respond appropriately to the rapid market changes of these new industries (Saxenian 1994). Small firm clusters are therefore perceived to represent the future optimal spatial and

organizational arrangements in industries with very short product life cycles (Piore and Sabel 1984; Porter 1990; Saxenian 1994).

Such arguments, however, are based on very strong assumptions about the relationship between information generation, information exchanges and geographical scales. Following Marshall (1920) and Vernon (1960), the clustering argument is based on the assumption that information spillovers are generated and realised specifically at the geographical scale of the local urban area. Urban clustering is therefore advantageous for industries which exhibit very short product life-cycles (Vernon 1966, 1979). Yet, recent research within the electronics and semiconductor industry (Suarez-Villa and Rama 1996; Suarez-Villa and Karlsson 1996; Wever and Stam 1988) suggests that agglomeration linkages, and the formal outcomes of any informal information spillovers (Audretsch and Feldman 1996; Suarez-Villa and Walrod 1997; Arita and McCann 2000) extend over much larger spatial scales than that of the individual urban metropolitan area. In the case of multi-plant multinational firms (Cantwell and Iammarino 2000), any such agglomeration effects may even operate over spatial scales larger than individual countries. These empirical observations therefore cast doubt on the assumed importance of specifically local inter-firm information spillovers as a source of competitive advantage (Porter 1990, 1998) within the electronics industry, and point rather more to the role of labour market hysteresis as a possible rationale for industrial clustering (Angel 1991; Arita and McCann 2000). More importantly, however, these observations also cast doubt on the whole hypothesis that small firm clusters represent something of an ideal spatial and organizational arrangement ensuring the maximization of innovation, either for the semiconductor industry or any other innovative industry facing short product life-cycles.

Part of the problem here is that so much of the literature which purports to show a high correlation between spatial industrial clustering, small and medium sized firms and short product life-cycles, has tended to focus on the spatial and organizational issues of only one particular part of the global electronics and semiconductor industry. The electronics industry as a whole is comprised of many sub-sectors ranging from the semiconductor industry to the consumer electronics sectors, and the semiconductor industry itself is comprised of three quite distinct sub-sectors, defined in terms of the nature of the activities and the transactions they undertake. Observations of Silicon Valley and the 'Cambridge Phenomenon' (Castells and Hall 1994) are actually primarily observations of groups of small firms whose activities correspond solely to only one of the three sub-sectors within the semiconductor industry, namely the Design sector. Yet, there are also many large vertically-integrated firms in this same sub-sector of the industry which are almost entirely ignored by the literature. Similarly, the other two parts of the semiconductor industry, the Wafer Process and the Wafer Manufacturing sectors, are characterized almost entirely by vertically-integrated wafer manufacturing and assembly firms. The spatial and organizational arrangements of the vertically-integrated parts of the semiconductor are completely different to the small semiconductor firms (Arita and McCann 2001). The relationships between geography and technology within the semiconductor must therefore be considered individually for each of the three sub-sectors of the industry. Only in this way can we assess whether or not the types of spatial and organizational arrangements of Silicon Valley are more generally applicable to the parts of the industry.

Firm location behaviour within the semiconductor industry is often the result of different, and sometimes conflicting objectives. Rarely is the geographical result in reality a Silicon Valley-style spatial clustering of highly innovative small firms generating very short product life-cycle outputs. This is partly why such high-technology clusters are of interest, but also it is why generalizations based on such observations should be avoided. In order to appreciate these points we must first discuss the nature and organization of the semiconductor industry itself.

### ***3. The Organization of the Semiconductor Industry***

In order to understand the organization of the semiconductor industry it is first necessary to understand the different activities which take place within the industry (Nishimura 1995, 1999; EIAJ 1994). As we see in Fig.1, the different activities in the semiconductor industry can be compared more or less directly with the different activities which take place in the book publishing industry.

**Fig.1.** Production Process of Semiconductor: Comparison with Book Publishing and Printing

The first stage of the production process is the silicon chip design stage, in which the functional logic of the chip, and three-dimensional circuit layout of transistors and capacitors within the silicon wafer is determined. This activity is carried out primarily using computer aided design (CAD) systems. This stage of the process can be compared with the planning, editing and layout stages of the book publishing process. The result of this stage is the production of masks, which are the three-dimensional templates of the chip. These Integrated Circuit (IC) design activities are undertaken both by the large number of small specialized IC design firms, and also by large vertically-integrated semiconductor producing firms. The activities are provided for by specialist CAD vendor firms which provide customized design software for the designers. At the same time, there has also emerged recently a sub-sector of the industry which is concerned only with the construction of intellectual property rights relating to IC designs. These firms design only logic functions without circuit layouts, and act in consultation with both small and large IC design firms in order to ensure patents are granted for the new chip protocol designs. The number of firms involved in this stage of the production process has grown enormously during the last two decades, with small design-oriented firms tending to be clustered in locations such as Silicon Valley. It is this part of the industry which has received so much academic attention. Yet, there are still many IC design activities which take place within vertically-integrated semiconductor producers both inside and outside of Silicon Valley.

The second stage of the process is the wafer process, the technology of which is determined by materials science. At this stage of the production process the circular silicon wafers, produced by specialist chemicals firms, are subjected to lithography. This is a process whereby ultra-violet light is used to illuminate certain parts of the wafer, according to the mask design, in order to bring about chemical changes within certain parts of the wafer. The wafers are then etched and treated, thereby removing the parts of the wafer subjected to the lithography. After as many as fifteen stages of lithography and treating, the

result is a three-dimensional silicon structure. This stage of the semiconductor production process can be compared to the plate-making and phototype process which takes place in the book printing industry.

The final stage of the wafer production process is that of the wafer assembly process. Here, the circular wafers which have been subjected to lithography and treating are extracted and dissected into many small square chips, each of which is then framed in plastic or ceramics for insulation and protection. This stage of the chip production process is the equivalent of the book binding process within the book publishing industry.

The level of technology of the second and third stages of the wafer and assembly process is defined in terms of the minimum processing rule and the wafer size. The minimum processing rule is the definition of the level of miniaturization of the technology, and the wafer size is the size of the individual silicon wafers which can be produced and then dissected to produce chips. The smaller is the minimum processing rule and the greater is the wafer size, the more advanced is the technological generation. In terms of technology, the second and third stages of the semiconductor production process are just as important to the semiconductor industry as the first stage, and the product life-cycles are just as short. Different minimum processing rules and wafer sizes represent completely different generations of technology.

The majority of these second and third stage activities tend to be carried out by two groups of firms in more geographically dispersed locations outside of the US (Arita and McCann 2001), and this may explain why these sectors have received relatively little academic interest. The first group of firms undertaking the wafer and assembly processes are the vertically-integrated semiconductor producers such as Intel and NEC, which undertake all of their own chip design and manufacturing activities. Firms such as NEC, Philips, Fujitsu and Motorola, which also manufacture finished goods, produce for internal demand as well as for other consumer firms, whereas firms such as Intel produce entirely for external customers. The common feature of the production of these firms is high volumes. The second group of firms undertaking the wafer and assembly processes are the specialist East Asian sub-contracting IC manufacturing firms. These are primarily Taiwanese, Japanese and Korean firms. They are comprised of a small number of specialist large firms, such as the Taiwan Semiconductor Manufacturing Company, which have both the capacity to produce ICs in large numbers, and also the technology to allow both the high degree production specificity and flexibility required to manufacture custom-designed ICs.

Having discussed the nature of the semiconductor industry, in the next section we will look at the relationship between technological change and spatial industrial organization in the case of the semiconductor manufacturers who are located in Japan, in order to assess whether the spatial and organizational arrangements here mirror those often observed in the literature on the US industry. In particular we will focus on those firms which carry out the second and third-stage wafer process and assembly activities. The object of this exercise is to assess the extent to which orthodox product life-cycle approaches can broadly account for the technology-space relationship in the Japanese sector.

#### ***4. Data and Methodology***

The data we employ comes from the 1999 Nikkei compendium of the semiconductor industry, and provides individual plant and production line data for every semiconductor firm located within Japan. The total number of such firms in Japan is 108, and these firms account for 509 individual plants. In terms of general establishment data, the Nikkei compendium provides us with the location details of each plant, the total employment levels of every plant, the actual floorspace of every production facility, and the total site area of a plant including areas external to the actual production activities. For technology indices, the Nikkei compendium provides us with information on the minimum processing rule and the wafer size of the products produced at each location. Nikkei also provide us with details of the wafer processing capacity of the plant. As far as we are aware, such detailed semiconductor technology data has never before been employed statistically by applied economists. These general establishment level data and plant technology indices are then combined with regional spatial data. The local wage indices we use are the average wages for each of the forty-six prefectures within Japan. These data come from the Japanese Office for Statistics. We also use a geographical information system to calculate the distance in kilometers between the location of the individual plant and the headquarters of its parent organization, and also the distance between the location of the individual plant and Tokyo. The number of establishments for which all of the individual plant, technology and regional data are complete is 106, and the data summary statistics are given in Table 1.

With our technology, plant and spatial data we can now begin to investigate the relationship between geography and the implementation of technology within the Japanese wafer processing component of the semiconductor industry. Following an orthodox product-cycle argument we can hypothesize that different generations of semiconductor technologies will be spatially differentiated within the Japanese semiconductor industry. In particular, we would expect that the most recently developed products requiring the most advanced, miniaturized and newer production technologies will tend to be implemented at more central locations. In terms of technology indices, more advanced generations of technology are represented by smaller minimum processing rules and larger wafer sizes. On the other hand, more mature vintages of product and process technologies would be expected to be implemented in more geographically peripheral locations exhibiting lower wage rates. The reason for this is that less advanced technology products will have become rather more standardized and easier to mass produce than more recent higher technology products. Moreover, increasing production quantities also implies the need for larger plants with larger land and labour requirements. This will provide an incentive for such plants to be located in lower wage and land price regions. Therefore, we ought to observe something of a negative correlation between the vintage of technology, the location of the product and process technology implementation and the level of peripherality of the establishment.

One issue which we need to consider is exactly what is meant by a 'central' location. In an orthodox product-cycle model we tend to think of a central location as being the dominant urban area (Vernon 1960, 1966) in which all of the major information-intensive activities of a particular sector or range of sectors are located. In the case of Japan, the urban area of Tokyo, known as the Kanto region, is very much the nationally-dominant

region of the economy, and regional wages and land prices generally fall with increasing distance away from Tokyo. Tokyo is therefore used as the reference point for our calculations of the level of peripherality of an individual plant. At the same time, in order to allow for the fact that within corporate structures a plant's dominant information networks may not necessarily be linked to the Tokyo region, we also will consider notions of peripherality defined with respect to the parent company's Japanese headquarters.

In order to test for an association between the level of geographical peripherality and the vintage of technology implemented we set up a series of multiple regression models. In Models 1 and 2 we choose as our dependent variable the distance between the individual plant and Tokyo, and we regress this against seven potential independent explanatory variables. These variables are the local prefecture wage, the number of plant employees, the overall plant site area, the actual production floorspace of the plant, the minimum processing rule, the wafer size, and the wafer processing capacity. From the product-cycle argument we would expect that the estimated coefficients will be positive for the employment, site area and floorspace variables, and negative for the minimum processing rule and wafer size indices. The estimated coefficient for the wafer processing capacity might be expected to be positive, on the grounds that a larger wafer processing capacity will require generally larger facilities. On the other hand, this can also be interpreted as a partial index of production technology, in which case the expected sign may be negative. In Models 3 and 4 we repeat the exercise having omitted certain explanatory variables. In Models 5 and 6 we repeat the exercise, but in these cases the dependent variable is the distance between the individual plant and the location of its parent headquarters. In order to allow for the fact that the direction of causality in the product life-cycle model is ambiguous, in Models 7 and 8 we re-estimate our technology-location regressions by using the minimum processing rule as the dependent variable and including distance as an independent explanatory variable.

#### **4. Results**

Our first model, Model 1 uses Ordinary Least Squares to estimate the relationship between the distance of the plant from Tokyo as a function of all the other seven variables. The results are given in Table 2. As we see from Table 2, the results for Model 1 appear to be rather poor, with only the local prefecture wage appearing significantly related to the level of geographic peripherality. Removing the non-significant explanatory variables and re-estimating this relationship in a stepwise manner as in Model 2 provides us with results described in Table 3. The performance of Model 2 improves only slightly after removing the non-significant variables in Model 1. However, in general, Models 1 and 2 only confirm the fact that the distance from Tokyo is negatively related to the local wage rate, which is a result we would expect to see in an economy with such a centre-periphery regional economic structure as Japan. There appears to be no relationship between centre-periphery location of the plant and the level of technology employed or implemented. In Model 3 we repeat the procedure of Model 1 but in Model 3 we have now removed floorspace as an explanatory variable because it is so highly correlated with the number of plant employees. The results for Model 3 are given in Table 4. As with Model 1, in Model 3 only the wage variable is significant. The results from Tables 2, 3 and 4 therefore all appear to suggest that there is no relationship between location of a plant and the level of technology



employed or implemented, at least where centrality and peripherality is defined with respect to Tokyo. The only confirmed relationship is the expected negative relationship between the level of geographical peripherality and the local wage rate.

As we have already mentioned, it may be argued that for plants within vertically-integrated corporate control and information networks, the reference point for notions of centrality will be the major decision-making centre of the corporate hierarchy. In order to account for this, we can re-estimate Model 1, but in Model 5 we use the distance between the plant and its parent headquarters' location as the measure of peripherality. In Table 5 we see that the local prefecture wage is still negatively associated with the distance from the plant to its headquarters, but this distance is also positively associated with the wafer processing capacity of the plant, which itself is a proxy for the plant size. Removing all of the non-significant variables in Model 5 and re-estimating the model with only these two significant parameters gives us Model 6, the results of which are described in Table 6. The results in Table 6 confirm that the local wage rate is negatively associated with the distance from the plant to its parent headquarters and also suggest that it is positively associated with the plant's wafer processing capacity. As with Model 3 above, however, we can remove floorspace as an independent explanatory variable from Model 5 because it is so highly correlated with employment, and then we re-estimate Model 5 as Model 7. From Table 7 we see that now the only significant variable at the five per cent level is that of the local wage, although the number of plant employees is significant at the 7 per cent level. The wafer processing capacity is now no longer significant, but the number of plant employees can also be interpreted as the best measure of the size of the facility. Once again, we can re-estimate Model 7 in a stepwise manner by removing each of the non-significant parameters. The results of the estimates of Model 8 are given in Table 8. The prefecture wage and the number of plant employees are negatively and positively correlated with the distance of the plant from its parent headquarters, respectively.

Each of the models so far has confirmed that there appears to be a negative relationship between the geographic peripherality of the location of the plant and the local wage rate, irrespective of whether location is defined with respect to Tokyo or the parent headquarters of the plant. At the same time, if we take the location of plant's parent headquarters as our geographical reference point for centrality, the size of the plant appears to be significantly related to the level of peripherality. However, for all of the models 1 to 7, there appears to be no significant relationship between the location of the production facility and either of the two measures the level of technology of the plants or the products being produced. In part this may be because there is no systematic direction of causality in product-cycle models between the location of the activity and the level of technology implemented. Therefore in order to allow for this problem of a lack of causality in product-cycle models we re-estimate the model using the minimum processing rule as the dependent variable, and investigating the extent to which it is a function of all the other spatial and non-spatial variables after removing the floorspace variable. The results to Model 9 are given in Table 9. As we see, the minimum processing rule, which is one of the two technological indices is only related to the wafer size, which itself is an index of technology. In other words, there appears to be no association between a plant's level of technology and any of the plant's geographical or production capacity variables. Removing

all of the non-significant variables and re-estimating Model 9 as Model 10 gives us the results in Table 10.

## **5. Discussion**

The evidence presented here suggests that there is little or no association between the level of technology implemented in a particular facility and the centrality of its geographical location within Japan. The very marked centre-periphery structure of the Japanese urban system appears to provide no clue as to the spatial distribution of technology within the Japanese wafer processing component of the semiconductor industry. The only evidence which appears to arise from the data is that larger plants tend to be located at greater distances from their parent headquarters and in lower wage regions, an observation which is consistent with orthodox location theory. These observations can be accounted for in two quite different ways. The first argument is to assume that the levels of technology implemented are more or less the same for all plants in the sample, and that we would therefore expect to see no systematic differences in the locations of the plants. However, as we have already explained, different minimum processing rules and wafer sizes represent different generations of technology in an industry in which miniaturization, and consequently increasing IC processing power, is the key defining feature of technological progress. The alternative explanation for our observations is that the spatial organization of production within Japan is quite different to that of the US. In particular, the Japanese semiconductor industry is comprised almost entirely of plants which are part of vertically-integrated hierarchical organizations. The relationship between technology and geography in this industry therefore depends on the spatial organization of these vertically-integrated firm hierarchies. These are points we will now consider.

In terms of their spatial-organizational characteristics, the vertically-integrated Japanese semiconductor producers can be split into two groups. The first group, are the firms whose headquarters are based in the Kanto region, and the second group are the firms from the Kansai region. Kanto and Kansai are the regions which contain the two largest urban concentrations in Japan, namely the Tokyo-Yokohama metropolitan area, and the Osaka-Kyoto-Kobe metropolitan area. All of the Japanese vertically-integrated semiconductor firms exhibit a similar, and very simple form of keiretsu organizational structure. The parent company generally has a series of plant locations at which high-level decision-making, research and product development take place. Within Japan, this first stage of the semiconductor production process, as described by Fig.1, tends to be situated geographically in the two major urban concentrations. Reporting directly to these plants is a second tier of plants, which consists of a series of wholly-owned subsidiary plants, almost all of which focus on the wafer process activity. Finally, there is a third tier of plants, which focus only on the wafer assembly process. The second and third stages of the semiconductor production process, which are the wafer processing and wafer assembly operations, take place in almost all central or peripheral areas of Japan. These affiliated wafer assembly plants, which may be either majority or wholly owned by the parent company, report directly to the second tier of plants, which themselves report directly to the top tier of plants. Only the higher level plants within the local groups generally report directly to the headquarters region, although there are a small number of geographically peripheral facilities which do report directly to the top level. Meanwhile, the overseas

plants of these vertically-integrated firms all report directly to the headquarters locations. This is because there is no particular local hierarchical organizational network between plants located in the same global region, as there is between the plants within the same Japanese regions.

**Fig.2** The Spatial Organization of Semiconductor Plants at Hitachi (1995).

**Fig.3** The Spatial Organization of Semiconductor Plants at Sony (1995).

**Fig.4** The Spatial Organization of Semiconductor Plants at Sharp(1995).

**Fig.5** The Spatial Organization of Semiconductor Plants at Rohm(1995).

The strict hierarchical organizational arrangements described above are largely replicated geographically. The higher level establishments are located in the two major urban concentrations, while the wafer plants and assembly plants are located in a variety of both central and peripheral locations. There is, however, a very particular logic to their spatial organization. The plants are often arranged into local spatial clusters in which groups of assembly plants are located close to the particular wafer process plant that they report to. Examples of four such firms Hitachi, Sony, Sharp and Rohm, are shown in Figs. 2-5. Each of these diagrams are compiled using data from *Sangyo Times* (1995) and the *Press Journal* (1995) which document all of the industry's plants by location, activity, and position within the corporate organizational hierarchy. All of the data for each of plants is 1995 data, which is the latest date for which complete information is available. As we see, Hitachi and Sony are firms whose higher level establishments are located in the Kanto region around Tokyo, while Sharp and Rohm are firms whose higher level establishments are located in the Kansai region of Osaka-Kyoto-Kobe. In the cases of Sharp, Rohm and Sony, whose organizational structures are very simple, the wafer plants, which represent the local clusters of assembly plants, report directly to each of the higher-level establishments. The second and third tier plants are generally in more peripheral locations than the first tier plants. On the other hand, the organizational structure of Hitachi is much more complex, with second and third tier plants located in both central and peripheral areas. This is typical in the Japanese semiconductor industry. The spatial organization of activities and the spatial implementation of technological innovations are determined primarily with respect to the organizational logic of the keiretsu systems. Moreover, such organizational issues are determined within a multi-product environment, in which corporate control is exercised with respect to the production of a range of different outputs for either intermediate or final consumption. These resulting spatial patterns of plants are therefore primarily the result of the need for coordination between the plants within a well-defined system of formal inter-plant relations (Arita and McCann 2000), and are not the result of informal information networks of the type often discussed in relation to the electronics industry (Saxenian 1994). This is also the case for the higher level establishments. The locations of the headquarters of each of these companies depends primarily on the initial location of the founding of the company. Although it may also be tempting to attribute the reasons for these particular location patterns to agglomeration considerations of information spillovers, along the lines of the Silicon Valley descriptions above, the argument cannot be sustained. This is because a great deal of internal secrecy surrounds the development of silicon wafers. Moreover, not only is internal secrecy a behavioural feature typical of many vertically-integrated firms (Simmie 1998), but Japanese firms in general are notoriously

secretive even in comparison to other hierarchical organizations. Therefore, any potential localization effects could only be possibly associated with labour market hysteresis impacts (Simpson 1992), rather than any than issues relating to information spillovers. This is also the case with the wafer and assembly plants.

The results of these various organizational issues, is that the spatial pattern of technological innovations and new-product implementations within the Japanese semiconductor industry, cannot be accounted for within a straightforward product-cycle framework. In Japanese industry, location issues are generally determined primarily with respect to organizational issues, which themselves are often quite different to the types of organizational arrangements typical in the US. The outcome of this is that observations based simply on the Silicon Valley semiconductor industry, or even on comparisons with the electronics industry of New England (Saxenian 1994), will therefore be of little or no analytical use when discussing the spatial behaviour of the Japanese components of the global semiconductor industry.

## ***7. Conclusions***

This paper has discussed the various sub-sectors of the semiconductor industry, and applied a simple product-cycle model to the case of the Japanese wafer-processing part of the industry. The models presented here find little or no association between the implementation of technological innovations and the location of the activity. There is some evidence for industrial clustering between local establishments, but this takes place within a tight organizational logic designed specifically to rule out information externalities (Arita and McCann 2001). The only evidence we do find is that the larger facilities will tend to be in the more geographically peripheral and lower wage and land-price regions, an observation consistent with orthodox location theory considerations. The explanation we offer for these observations is that the spatial patterns of production in the Japanese semiconductor industry, are dominated by issues of decision-making and control within vertically-integrated hierarchical organizations. These particular types of hierarchical corporate relationships and also these particular types of local wafer process-assembly plant organizational arrangements, only exist in Japan and within the individual keiretsu groupings. The arguments presented here suggest that the location behaviour of these vertically-integrated parts of the global semiconductor industry are governed primarily by traditional multiplant and multinational location considerations, in which different activities or groups of activities are located in different regions for different reasons, subject to the organizational arrangements of the firm. Observations contrasting the behaviour of Silicon Valley and other parts of the semiconductor industry (Saxenian 1994) are of very limited analytical use for more general industry-organization discussions.

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	Mean	Standard Deviation
Distance from the plant to Tokyo (km)	341.474	276.894
Wage (Yen)	525223.83	119661.29
Plant Employees	1416.26	1540.20
Site Area (sq m)	136558.79	172308.96
Floorspace (sq m)	55732.99	58352.04
Minimum Processing Rule (um)	0.8289	0.7126
Wafer Size (mm)	150.00	40.82
Wafer Processing Capacity (per month)	21321.20	21185.90

**Table 1** Data Definitions and Descriptive Statistics

Parameter	Coefficient Estimate	t-statistic	Significance
Dependent Variable: Distance from Plant to Tokyo			
Constant	907.478	4.881	0.000
Wage	-0.458	-4.483	0.000
Plant Employees	0.028	0.195	0.846
Site Area	-0.016	-0.0162	0.0872
Floorspace	0.102	0.694	0.490
Minimum Processing Rule	0.007	0.063	0.950
Wafer Size	-0.119	-0.947	0.346
Wafer Processing Capacity	0.171	1.475	0.144
Adjusted R square	0.195		

**Table 2.** Results for Model 1

Parameter	Coefficient Estimate	t-statistic	Significance
Dependent Variable: Distance from Plant to Tokyo			
Constant	882.486	8.027	0.000
Wage	-0.458	-5.110	0.000
Adjusted R square	0.211		

**Table 3.** Results for Model 2



<b>Parameter</b>	<b>Coefficient Estimate</b>	<b>t-statistic</b>	<b>Significance</b>
Dependent Variable: Distance from Plant to Tokyo			
Constant	963.907	5.498	0.000
Wage	-0.446	-4.638	0.000
Plant Employees	0.125	1.328	0.187
Site Area	-0.012	-0.132	0.895
Minimum Processing Rule	0.038	-0.352	0.726
Wafer Size	-0.119	-0.947	0.346
Wafer Processing Capacity	0.110	0.990	0.324
Adjusted R square	0.180		

**Table 4.** Results for Model 3

<b>Parameter</b>	<b>Coefficient Estimate</b>	<b>t-statistic</b>	<b>Significance</b>
Dependent Variable: Distance from Plant to HQ			
Constant	843.460	4.734	0.000
Wage	-0.552	-5.992	0.000
Plant Employees	0.086	0.675	0.501
Site Area	0.023	0.257	0.797
Floorspace	0.035	0.263	0.793
Minimum Processing Rule	0.031	0.300	0.765
Wafer Size	0.000	0.002	0.999
Wafer Processing Capacity	0.200	1.911	0.059
Adjusted R square	0.346		

**Table 5.** Results for Model 5

<b>Parameter</b>	<b>Coefficient Estimate</b>	<b>t-statistic</b>	<b>Significance</b>
Dependent Variable: Distance from Plant to HQ			
Constant	842.356	7.036	0.000
Wage	-0.516	-6.020	0.000
Wafer Processing Capacity	0.220	2.568	0.012
Adjusted R square	0.369		

**Table 6.** Results for Model 6

<b>Parameter</b>	<b>Coefficient Estimate</b>	<b>t-statistic</b>	<b>Significance</b>
Dependent Variable: Distance from Plant to HQ			
Constant	909.687	5.188	0.000
Wage	-0.542	-6.169	0.000
Plant Employees	0.157	1.830	0.070
Site Area	-0.017	-0.207	0.837
Minimum Processing Rule	0.029	-0.287	0.775
Wafer Size	-0.030	-0.271	0.787
Wafer Processing Capacity	0.157	1.543	0.126
Adjusted R square	0.316		

**Table 7.** Results for Model 7

<b>Parameter</b>	<b>Coefficient Estimate</b>	<b>t-statistic</b>	<b>Significance</b>
Dependent Variable: Distance from Plant to HQ			
Constant	996.209	9.147	0.000
Wage	-0.589	-7.212	0.000
Plant Employees	0.178	2.183	0.031
Adjusted R square	0.326		

**Table 8.** Results for Model 8

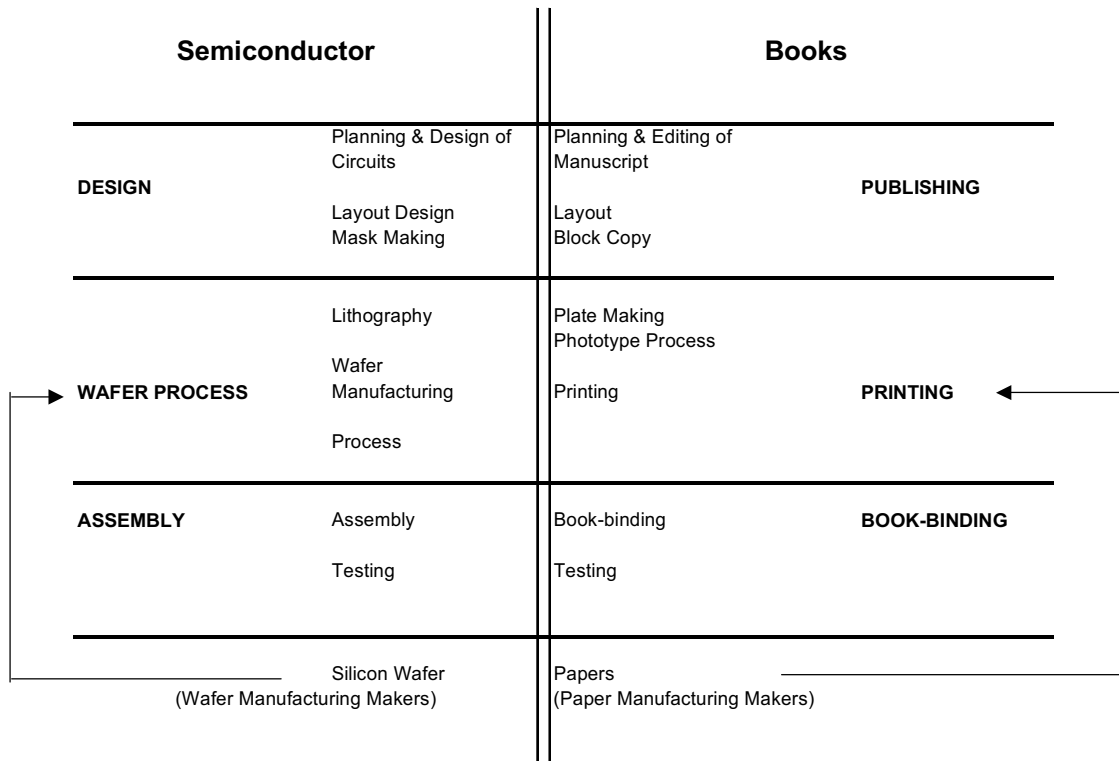
<b>Parameter</b>	<b>Coefficient Estimate</b>	<b>t-statistic</b>	<b>Significance</b>
Dependent Variable: Minimum Processing Rule			
Constant	2.339	5.516	0.000
Wage	-0.020	-0.207	0.836
Plant Employees	-0.054	0.616	0.539
Site Area	0.040	0.481	0.632
Distance from Plant from Tokyo	0.033	-0.352	0.726
Wafer Size	-0.504	-5.074	0.000
Wafer Processing Capacity	-0.120	-1.176	0.242
Adjusted R square	0.304		

**Table 9.** Results for Model 9

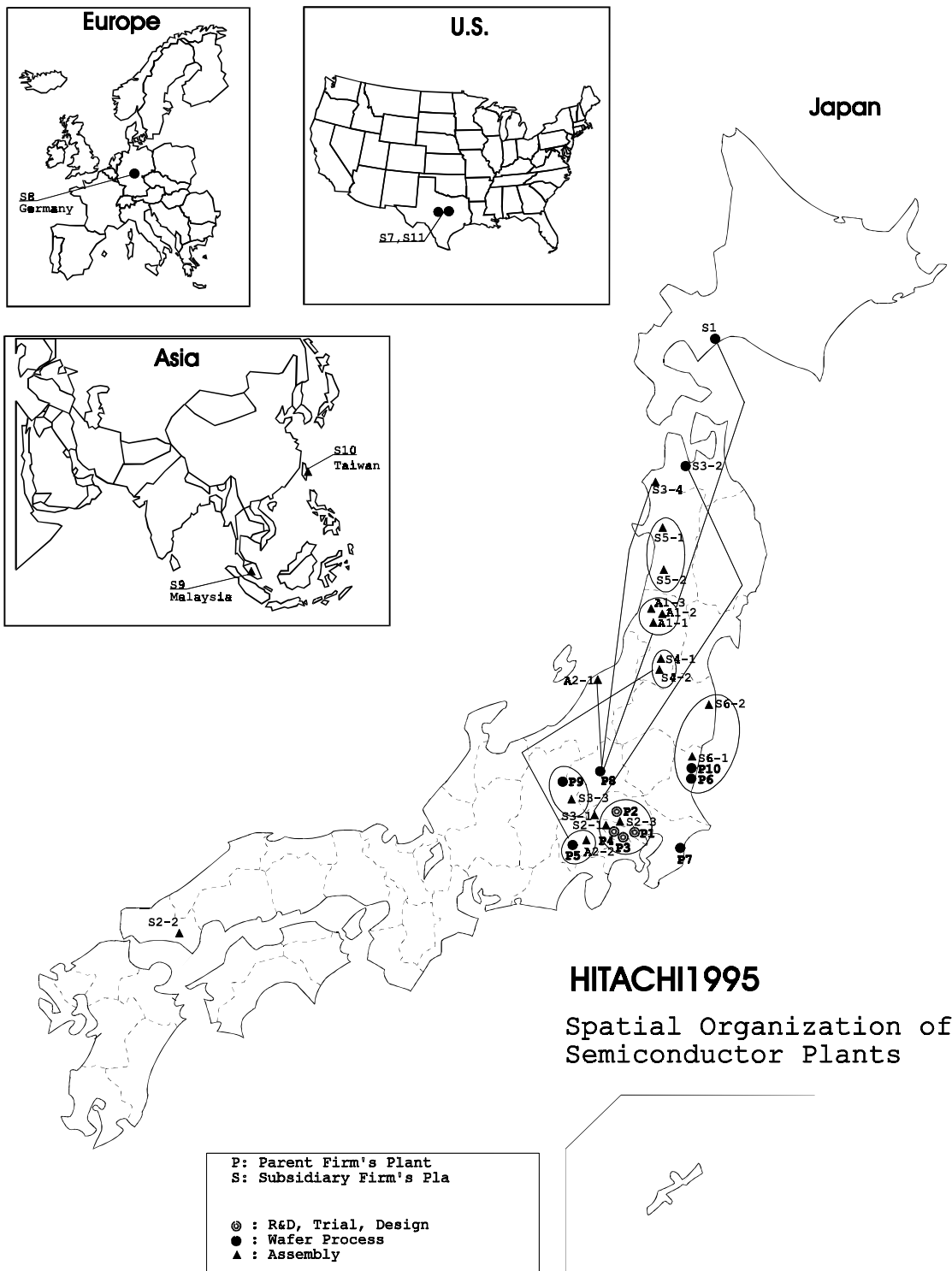
Parameter	Coefficient Estimate	t-statistic	Significance
Dependent Variable: Minimum Processing Rule			
Constant	2.327	10.666	0.000
Wafer size	-0.572	-7.114	0.000
Adjusted R square	0.321		

**Table 10.** Results for Model 10

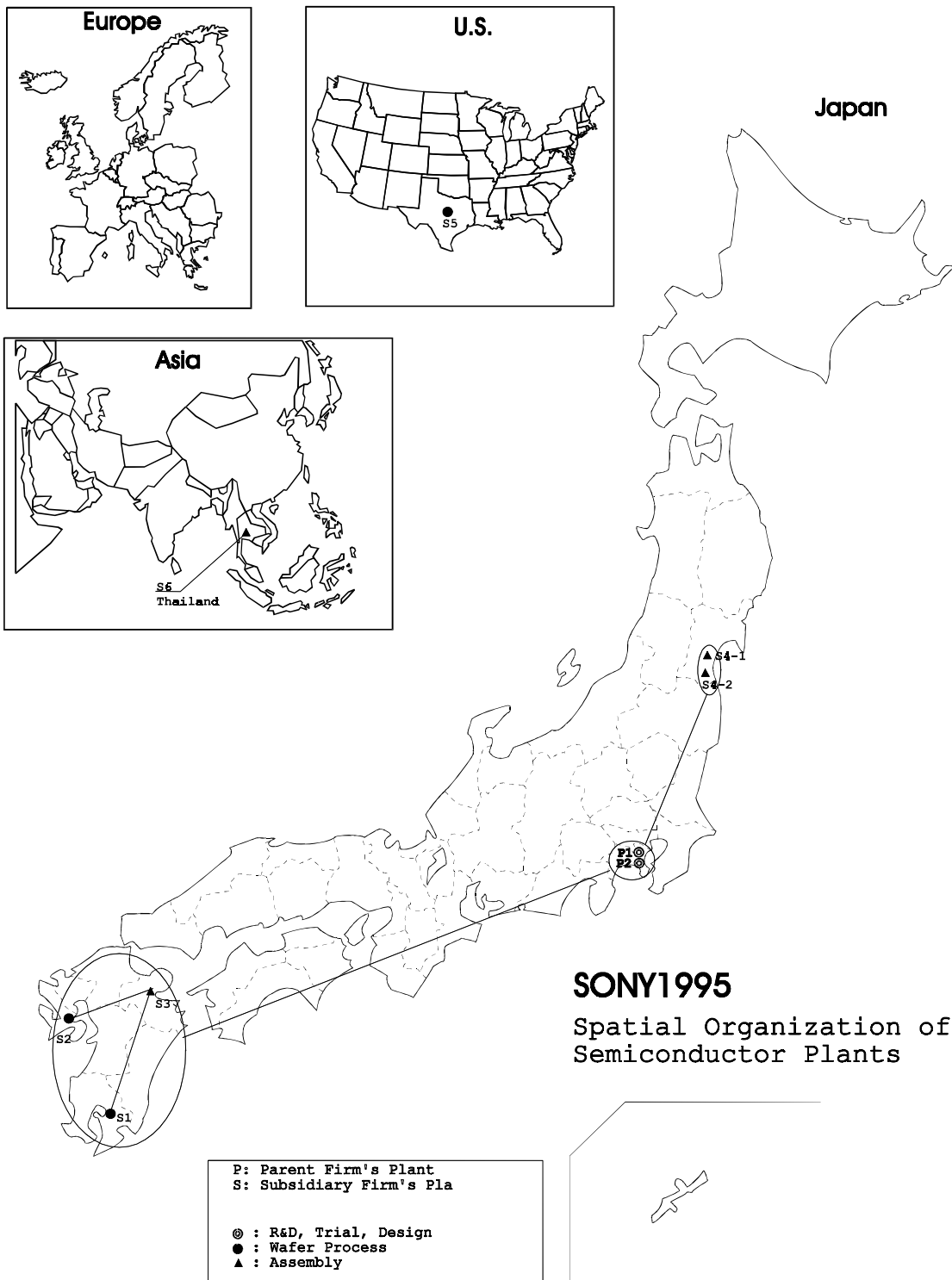
**Production Process of Semiconductor  
Comparison with Publishing and Printing**



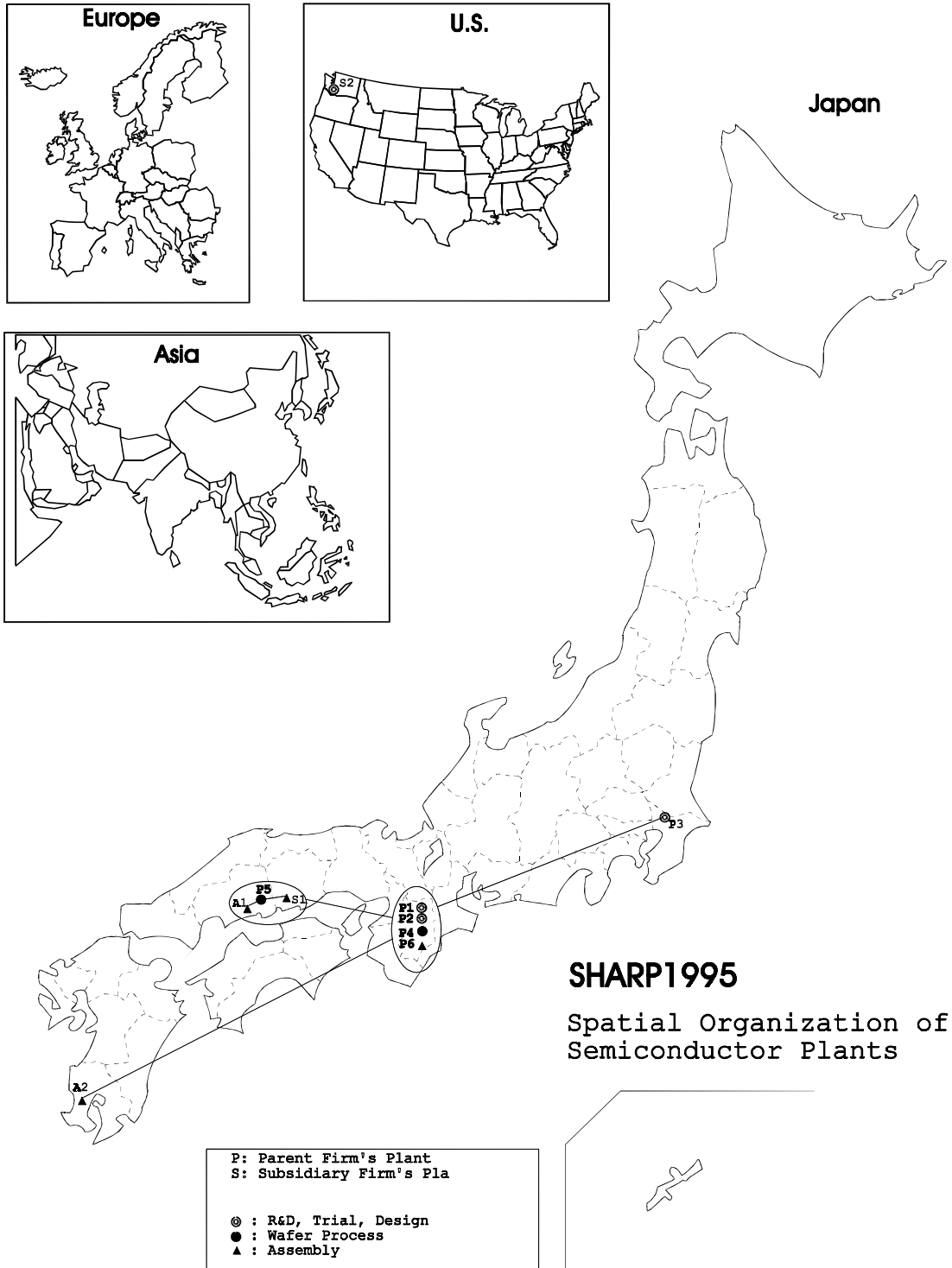
**Fig.1.** Production Process of Semiconductor: Comparison with Book Publishing and Printing



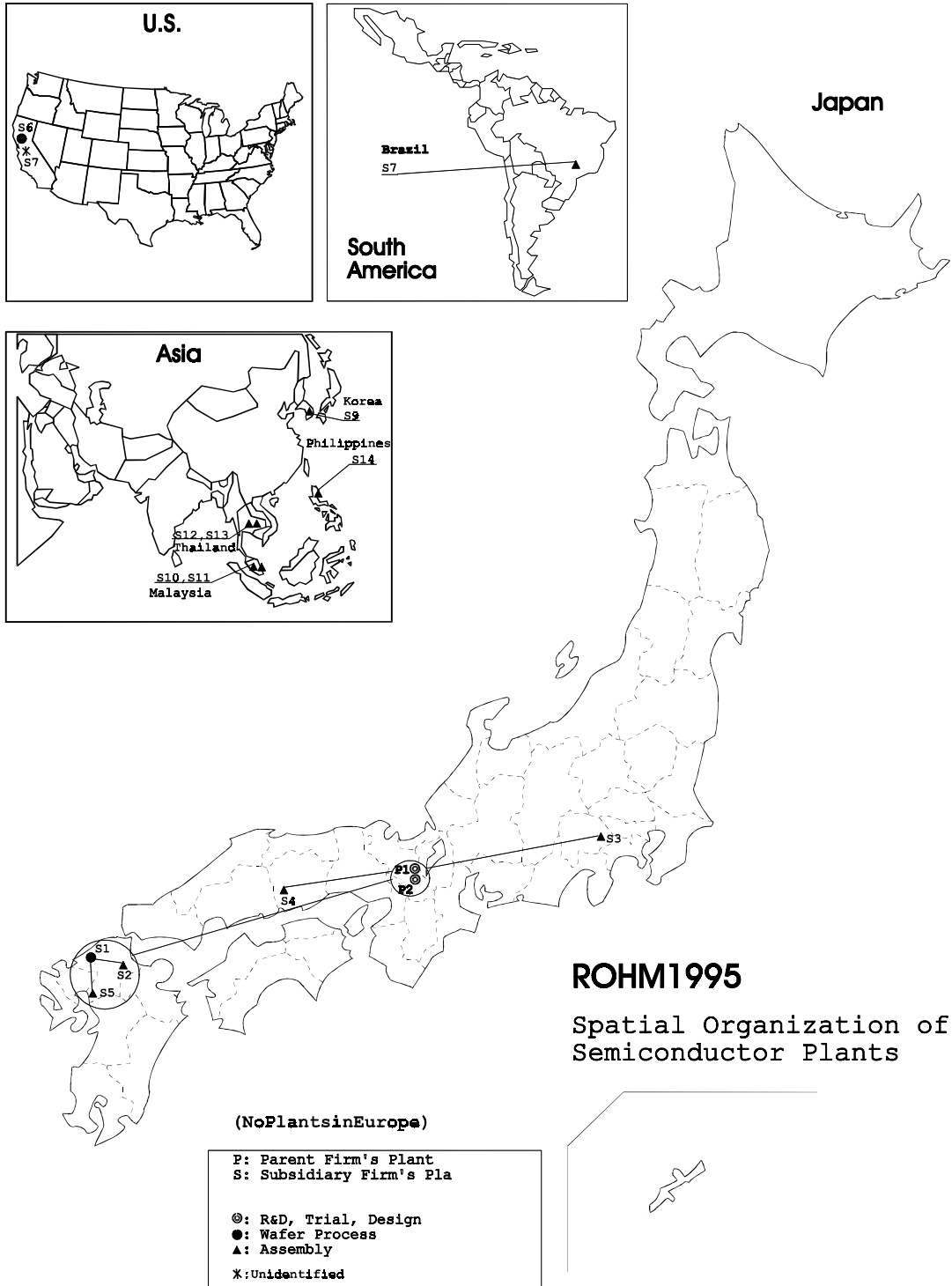
**Fig.2** The Spatial Organization of Semiconductor Plants at Hitachi (1995).



**Fig.3** The Spatial Organization of Semiconductor Plants at Sony (1995).



**Fig.4** The Spatial Organization of Semiconductor Plants at Sharp(1995).



**Fig.5** The Spatial Organization of Semiconductor Plants at Rohm(1995).